MICROWAVE POWER GaN MMIC DIE

JS9U29-AS

Preliminary

FEATURES

- **X-BAND 2-STAGE POWER AMPLIFIER**
- **HIGH POWER**
  Pout= 41.0dBm(Typ.) at 9.0GHz to 10.0GHz
- **HIGH GAIN**
  GL= 20dB(Typ.)
- **HIGH EFFICIENCY**
  PAE= 47%(Typ.)
- **PULSE OPERATION**
  Pulse width=100μs, Duty cycle=10%

RF PERFORMANCE SPECIFICATIONS (Ta= 25°C)

CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT	MIN.	TYP.	MAX.
Peak Output Power *1	Pout	VDD = 28V IDDset= 0.42A @Pin= 26dBm *1 f= 9.0 to 10.0GHz *2 f= 8.0 to 11.0GHz	dBm	—	41.0	—
Peak Output Power *2	Pout		dBm	—	40.0	—
Drain Current	IDD		A	—	—	1.0
Power Added Efficiency	ηadd		%	—	47	—
Linear Gain	GL	@Pin= 0dBm	dB	—	22	—

ABSOLUTE MAXIMUM RATINGS (Ta= 25°C)

CHARACTERISTICS	SYMBOL	UNIT	RATING
Drain- Source Voltage	VDD	V	35
Gate- Source Voltage	VGG	V	-4
Drain Current	IDD	A	TBD
Case Temperature	Tc	°C	-40 to +90
Input Power	Pin	dBm	TBD

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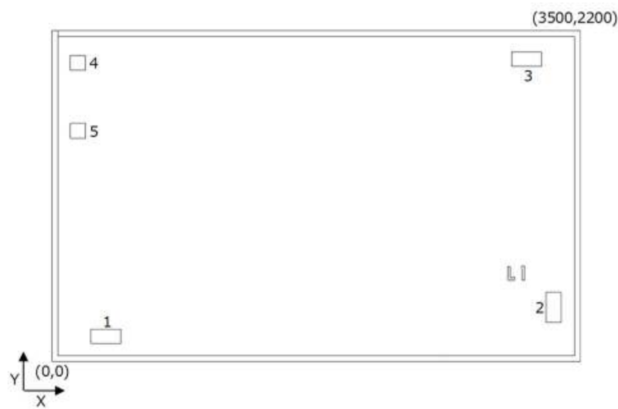
MECHANICAL INFORMATION

Die Size: 3.5mm × 2.2mm
Unit (inside a picture & a table): microns
Thickness: 100(+/-5)
Die size tolerance: +/-50
Ground is backside of die



Bond Pad Description

Pad No.	Symbol	Pad center position (um)		Pad size (um)		Description
		X	Y	X	Y	
1	RFin	356	168	200	96	RF input. Matched to 50 ohm. DC blocked.
2	VD2	3322	361	100	200	Drain voltage for stage 2.
3	RFout	3144	2009	200	96	RF output. Matched to 50 ohm. DC blocked.
4	VD1	172	1985	100	100	Drain voltage for stage 1.
5	VG	172	1534	100	100	Gate voltage for all stages.

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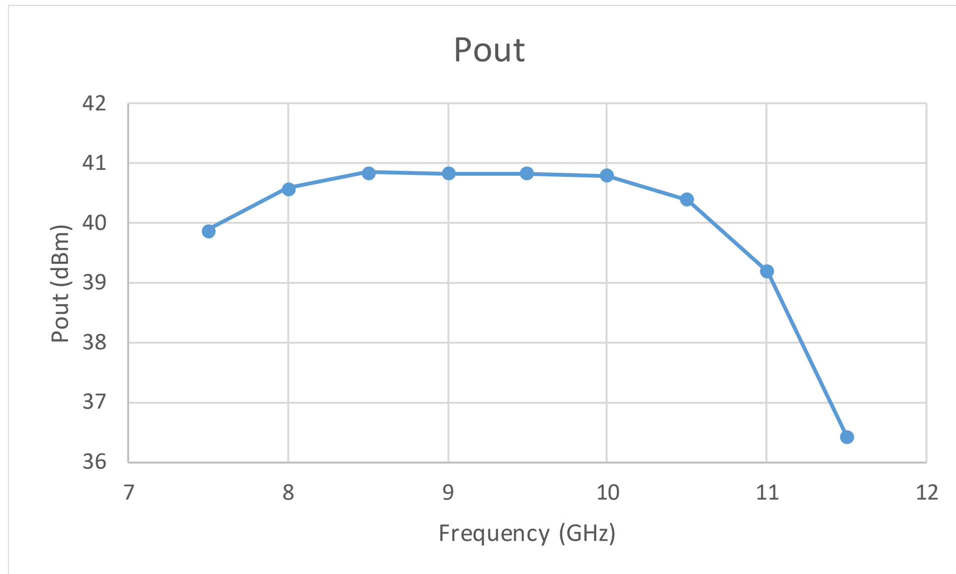
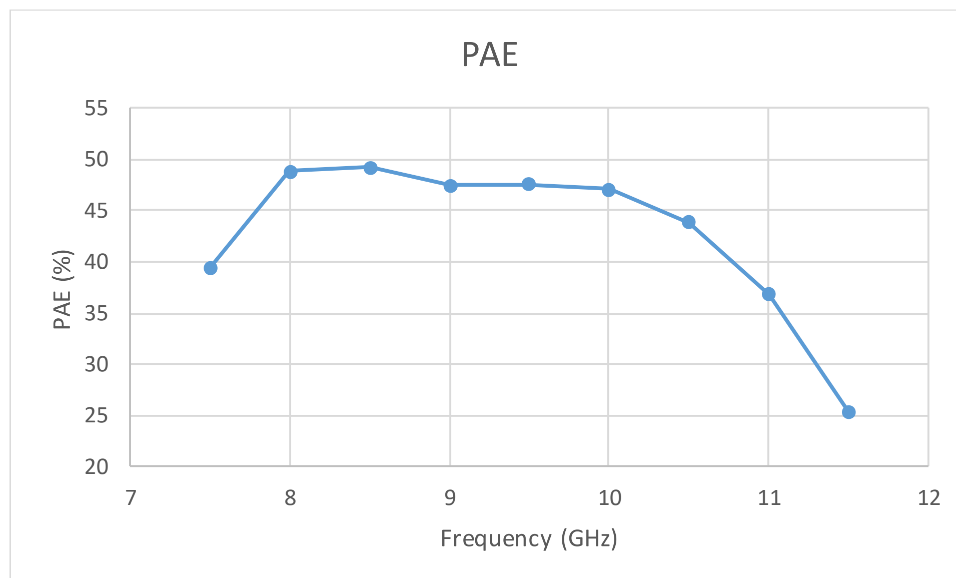
TYPICAL RF PERFORMANCE

·Pout , PAE vs. Frequency

VDD= 28 V (pulsed), IDDset= 0.42 A, Pin = 26dBm, PW = 100μs, Duty = 10%, Ta= +25°C,

On wafer measurement





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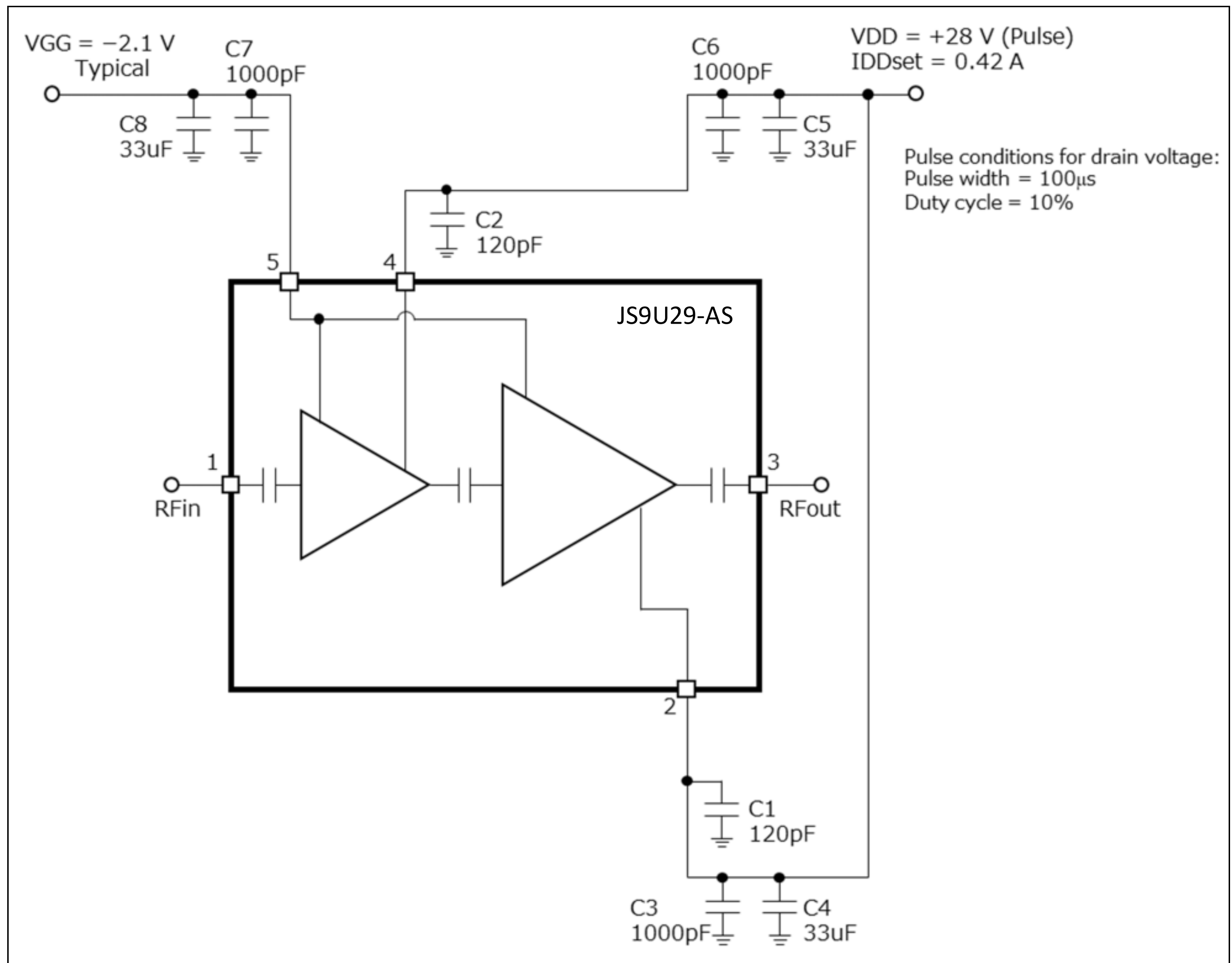
APPLICATION CIRCUIT



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STORAGE ENVIRONMENT

Three months under the following conditions
-temperature : 20°C to 27°C
-atmosphere: in dry nitrogen

RECOMMENDED ASSEMBLY METHODS

- Vacuum pencils and/or vacuum collets are the preferred methods of pick up.
- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- Devices must be stored in a dry nitrogen atmosphere.
- Thermosonic ball or wedge bonding are the preferred connection methods.
- 20-micron gold wire must be used for connections.

RECOMMENDED BIASING PROCEDURES

Bias Up Procedure

1. Set IDD limit to 1.5 A, IGG limit to 5 mA
2. Set VGG to −5.0 V
3. Set VDD +28 V
4. Adjust VG more positive until IDQ = 0.42 A (VGG ~ −2.1 V Typical)
5. Apply RF signal

Bias Down Procedure

1. Turn off RF signal
2. Reduce VGG to −5.0 V. Ensure IDQ ~ 0 mA
3. Set VDD to 0 V
4. Turn off VDD supply
5. Turn off VGG supply

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