# MICROWAVE POWER GaN MMIC DIE

# JS9U30-AS

**Preliminary**

## FEATURES

**·X-BAND 3-STAGE POWER AMPLIFIER**

**·HIGH POWER**

Pout= 44.0dBm(Typ.) at 9.0GHz to 10.0GHz

**·HIGH GAIN**

GL= 30dB(Typ.)

**·HIGH EFFICIENCY**

PAE= 45%(Typ.)

**·PULSE OPERATION**

Pulse width=100μs, Duty cycle=10%

## RF PERFORMANCE SPECIFICATIONS ( Ta= 25°C )

| CHARACTERISTICS | SYMBOL | CONDITIONS | UNIT | MIN. | TYP. | MAX. |
|---|---|---|---|---|---|---|
| Peak Output Power *1 | Pout | VDD = 30V<br>IDDset= 0.90A<br>@Pin= 22dBm<br>*1 f= 9.0 to 10.0GHz<br>*2 f= 8.0 to 11.0GHz | dBm | — | 44.0 | — |
| Peak Output Power *2 | Pout | | dBm | — | 43.0 | — |
| Drain Current | IDD | | A | — | — | 2.5 |
| Power Added Efficiency | ηadd | | % | — | 45 | — |
| Linear Gain | GL | @Pin= 0dBm | dB | — | 28 | — |

## ABSOLUTE MAXIMUM RATINGS ( Ta= 25°C )

| CHARACTERISTICS | SYMBOL | UNIT | RATING |
|---|---|---|---|
| Drain- Source Voltage | VDD | V | 35 |
| Gate- Source Voltage | VGG | V | -4 |
| Drain Current | IDD | A | TBD |
| Case Temperature | Tc | °C | -40 to +90 |
| Input Power | Pin | dBm | TBD |

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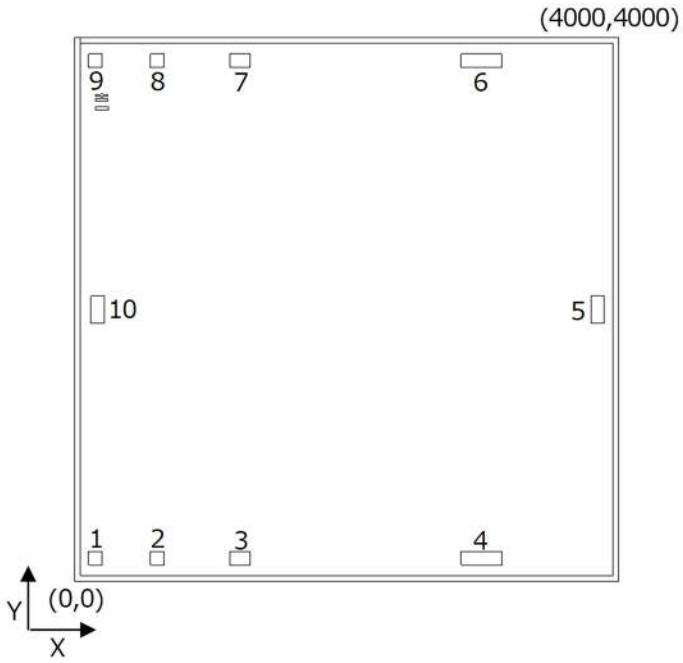
## MECHANICAL INFORMATION

Die Size: 4.0mm × 4.0mm
Unit (inside a picture & a table): microns
Thickness: 100(+/-5)
Die size tolerance: +/-50
Ground is backside of die




Bond Pad Description

| Pad No. | Symbol | Pad center position (um) | | Pad size (um) | | Description |
|---|---|---|---|---|---|---|
| | | X | Y | X | Y | |
| 1 | VGA | 152 | 172 | 100 | 100 | Gate voltage for all stages. |
| 2 | VD1A | 608 | 172 | 100 | 100 | Drain voltage for stage 1. |
| 3 | VD2A | 1216 | 172 | 150 | 100 | Drain voltage for stage 2. |
| 4 | VD3A | 2992 | 172 | 300 | 100 | Drain voltage for stage 3. |
| 5 | RFout | 3847 | 2000 | 96 | 200 | RF output. Matched to 50 ohm. DC blocked. |
| 6 | VD3B | 2992 | 3828 | 300 | 100 | Drain voltage for stage 3. |
| 7 | VD2B | 1216 | 3828 | 150 | 100 | Drain voltage for stage 2. |
| 8 | VD1B | 608 | 3828 | 100 | 100 | Drain voltage for stage 1. |
| 9 | VGB | 152 | 3828 | 100 | 100 | Gate voltage for all stages. |
| 10 | RFin | 170 | 2000 | 96 | 200 | RF input. Matched to 50 ohm. DC blocked. |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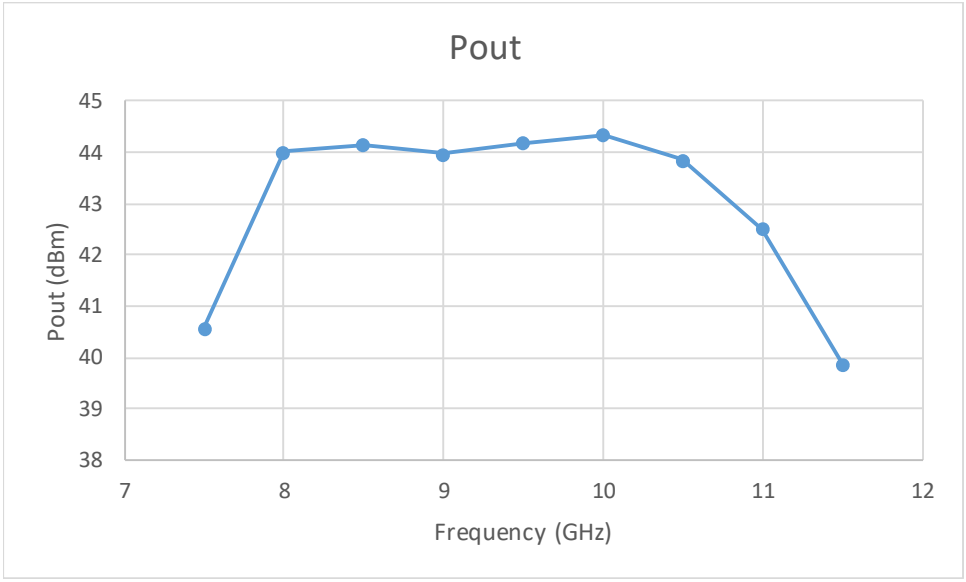
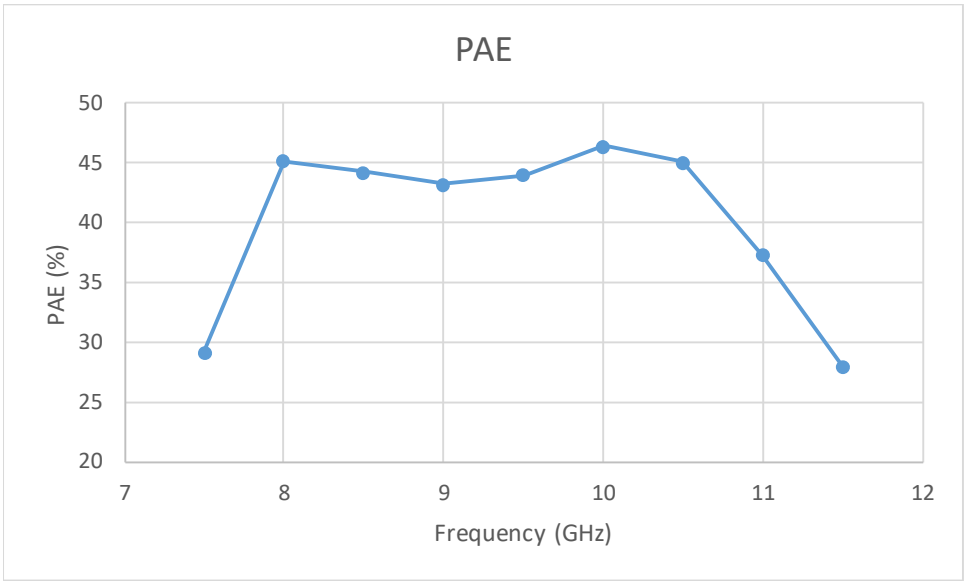
## TYPICAL RF PERFORMANCE

**·Pout , PAE vs. Frequency**

VDD= 30 V (pulsed), IDDset= 0.90 A, Pin = 22dBm, PW = 100μs, Duty = 10%, Ta= +25°C,
On wafer measurement





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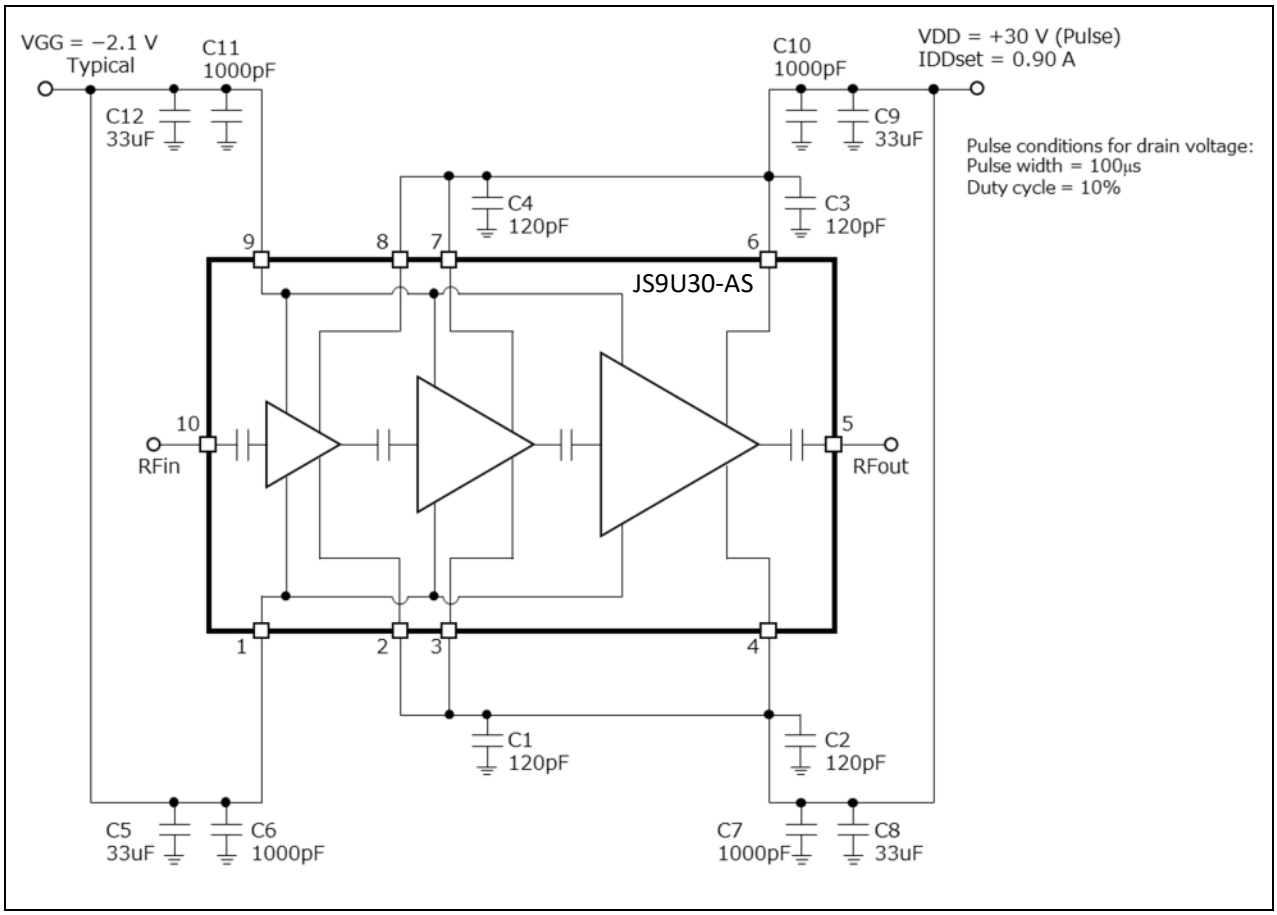
## APPLICATION CIRCUIT





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## STORAGE ENVIRONMENT

Three months under the following conditions
-temperature : 20°C to 27°C
-atmosphere: in dry nitrogen

## RECOMMENDED ASSEMBLY METHODS

- Vacuum pencils and/or vacuum collets are the preferred methods of pick up.
- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- Devices must be stored in a dry nitrogen atmosphere.
- Thermosonic ball or wedge bonding are the preferred connection methods.
- 20-micron gold wire must be used for connections.

## RECOMMENDED BIASING PROCEDURES

Bias Up Procedure
1. Set IDD limit to 3.0 A, IGG limit to 15 mA
2. Set VGG to −5.0 V
3. Set VDD +30 V
4. Adjust VG more positive until IDQ = 0.90 A (VGG ~ −2.1 V Typical)
5. Apply RF signal

Bias Down Procedure
1. Turn off RF signal
2. Reduce VGG to −5.0 V. Ensure IDQ ~ 0 mA
3. Set VDD to 0 V
4. Turn off VDD supply
5. Turn off VGG supply


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